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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/765,619	01/27/2004	Kie Y. Ahn	1303.033US2	1360

21186 7590 12/10/2004

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
P.O. BOX 2938
MINNEAPOLIS, MN 55402

EXAMINER	
SARKAR, ASOK K	

ART UNIT	PAPER NUMBER
2829	

DATE MAILED: 12/10/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/765,619	AHN ET AL.	
	Examiner	Art Unit	
	Asok K. Sarkar	2829	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-34* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1/27/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 14 – 18 are rejected under 35 U.S.C. 102(e) as being anticipated by Osten, US 2003/0193061.

Regarding claim 14, Osten teaches a transistor comprising:

- a body region 22 located between the first and second source/drain regions 18 and 20 (see Fig. 9);
- a praseodymium oxide dielectric layer 14 on the body region 22 (see Fig. 9); and
- a gate 16 on the praseodymium oxide dielectric layer 14 (see Fig. 9) in paragraphs 53 and 54.

The limitations that the praseodymium oxide dielectric layer is formed by a process including: evaporation depositing a praseodymium (Pr) metal layer on the body region and oxidizing the Pr metal layer to form the praseodymium oxide dielectric layer on the body region were not given any weight because the claim is a product by process claim.

Note that a "product by process" claim is directed to the product per se, no matter how actually made, *In re Hirao*, 190 USPQ 15 at 17 (footnote 3). See also *In re Brown,* 173

USPQ 685; *In re Luck*, 177 USPQ 523; *In re Fessmann*, 180 USPQ 324; *In re Avery*, 186 USPQ 161; *In re Wertheim*, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); *In re Marosi et al*, 218 USPQ 289; and particularly *In re Thorpe*, 227 USPQ 964, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. Note that applicant has the burden of proof in such cases, as the above case laws make clear.

Regarding claim 15, Osten teaches praseodymium oxide dielectric layer has an equivalent oxide thickness (EOT) of less than 2 nm in paragraph 13.

Regarding claims 16 – 18, Osten teaches forming very pure praseodymium oxide dielectric layer with reference to X-ray and TEM studies in paragraph 45. The process of making the praseodymium oxide dielectric layer is not considered because the claims are considered product by process claims (see explanation regarding claim 14 rejection).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.

4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

5. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

6. Claims 1 – 13 and 19 – 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Osten, US 2003/0193061 in view of Wilk, US 6,258,637 and Borden, US 6,154,280.

Regarding claims 1, 7 and 11, Osten teaches a transistor comprising:

- a body region 22 located between the first and second source/drain regions 18 and 20 (see Fig. 9);
- a praseodymium oxide dielectric layer 14 on the body region 22 (see Fig. 9), the praseodymium oxide dielectric layer has a dielectric constant of about 31 (see paragraph 13); and
- a gate 16 on the praseodymium oxide dielectric layer 14 (see Fig. 9) in paragraphs 53 and 54.

The limitations that the praseodymium oxide dielectric layer is formed by a process including: evaporation depositing a praseodymium (Pr) metal layer on the body

region by EB evaporation and oxidizing the Pr metal layer by Kr/O_2 plasma process to form the praseodymium oxide dielectric layer on the body region were not given any weight because the claim is a product by process claim.

Note that a "product by process" claim is directed to the product per se, no matter how actually made, *In re Hirao*, 190 USPQ 15 at 17 (footnote 3). See also *In re Brown,* 173 USPQ 685; *In re Luck*, 177 USPQ 523; *In re Fessmann*, 180 USPQ 324; *In re Avery*, 186 USPQ 161; *In re Wertheim*, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); *In re Marosi et al*, 218 USPQ 289; and particularly *In re Thorpe*, 227 USPQ 964, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. Note that applicant has the burden of proof in such cases, as the above case laws make clear.

Osten teaches the surface roughness of the dielectric layer in paragraph 33, but fails to teach that the surface portion of the body region has a surface roughness of approximately 0.6 mn.

Wilk teaches that the interface between the gate dielectric and the substrate should be as low as 0.05 nm in column 1, line 67 for the benefit of providing high device reliability and performance in column 1, lines 50 – 52.

Borden teaches that the roughness of the surface underneath the gate insulating layer should be about 0.1 nm (1 angstrom) for the benefit of the transistor being capable of withstanding higher electric fields in column 4, lines 29 – 40.

Therefore, it would have been obvious to one with ordinary skill in the art at the time of the invention to modify Osten and provide a surface portion of the body region that has a surface roughness of approximately 0.6 nm for the benefit of providing high device reliability and performance as taught by Wilk in column 1, lines 50 – 52 and also for the benefit of the transistor being capable of withstanding higher electric fields as

taught by Borden in column 4, lines 29 – 40.

Regarding claims 2 and 8, Osten fails to teach body region oriented in a (100) crystalline plane.

Wilk teaches (100) Si substrate in column 3, line 51 as a substrate for fabricating microelectronic circuits.

Therefore, it would have been obvious to one with ordinary skill in the art at the time of the invention to modify Osten and provide a substrate with body region oriented in a (100) crystalline plane since such substrates are used as a substrate for fabricating microelectronic circuits as taught by Wilk in column 3, line 51.

Regarding claims 3 and 9, Osten teaches body region oriented in a (111) crystalline plane in paragraph 24.

Regarding claims 4 and 10, Osten teaches praseodymium oxide dielectric layer is substantially amorphous in paragraph 10.

Regarding claims 5 and 6, Osten teaches forming very pure praseodymium oxide dielectric layer with reference to X-ray and TEM studies in paragraph 45. Osten fails to teach the dielectric layer is without silicon oxide or silicide.

However, it would have been obvious to one with ordinary skill in the art at the time of the invention that the dielectric layer is not contaminated with silicon oxide or silicide since the crystalline and the diffraction properties will be changed due to the contamination of impurity phases especially in the electron diffraction results.

Regarding claims 19 – 26, Osten teaches a memory devices that includes access transistors in paragraph 3 and most limitations have been described earlier in rejecting claims 1, 4 – 7 and 10 – 18.

7. Claims 27 – 34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Osten, US 2003/0193061 in view of Wilk, US 6,258,637; Borden, US 6,154,280 and the Admitted prior Art (APA).

Osten in view of Wilk and Borden teaches most limitations of these claims as Described earlier in rejecting claims 1 – 25.

Osten in view of Wilk and Borden fails to teach an information handling devices such as computer having a processor, wordlines, sourcelines, bitlines and a system bus coupling the processor to the memory device.

The APA teaches that the transistor and the memory devices can be used in an information handling devices such as computer having a processor, wordlines, sourcelines, bitlines and a system bus coupling the processor to the memory device and is well known in the art in descriptions of pages 11 and 12.

Therefore, it would have been obvious to one with ordinary skill in the art at the time of the invention to use the devices taught by Osten in view of Wilk and Borden in an information handling devices such as computer having a processor, wordlines, sourcelines, bitlines and a system bus coupling the processor to the memory device since it is well known in the art to use these devices in a computer as taught by the APA in pages 11 and 12.

Conclusion

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Asok K. Sarkar whose telephone number is 571 272 1970. The examiner can normally be reached on Monday - Friday (8 AM- 5 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Tokar can be reached on 571 272 1812. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

9. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Asok Kumar Sarkar

Asok K. Sarkar
November 30, 2004

Patent Examiner